In the Claims:

Please amend the claims as shown:

1-117 (Cancelled)

118 - 121 (Cancelled)

122. (Currently Amended) ~~An arithmetic~~ A method for coding input image data in a predetermined signal format, comprising:

~~by~~ dividing said image data into block units; and

~~by~~ carrying out orthogonal ~~transform~~ transformation in said block units ~~or for subjecting coded data to inverse orthogonal transform and signal format conversion to obtain image data for decoding~~ at a time when data output value ~~Y0, i.e.,~~ X0 + X1 , and data output value ~~Y1, i.e.,~~ X0 - X1 , are generated from two data input values X0 and X1 by at least a function of said orthogonal transform transformation ~~or said inverse orthogonal transform~~, said coding method comprising the following steps:

~~first, a subtraction step for subtracting said X1 from said X0 to generate new X0,~~

~~second, a twice value generating step for generating new X1 being twice the value of said X1, and~~

~~third, an addition step for adding said new X0 to newer X1 to generate new X1, wherein~~

~~said newer X1 is used as output value Y0, and said new X0 is used as output value Y1~~

setting said X0 value in a register A and setting said X1 value in a register B;

subtracting said X1 value from said X0 value to obtain a new X0 value and storing said new X0 value in register A;

shifting said X1 value used as a binary number by one bit to a MSB side to obtain a new X1 value and storing said new X1 value in register B;

adding said new X0 value to said new X1 value to obtain a further new X1 value and outputting said further new X1 value as a sum of said new X0 value and said new X1 value.

123 - 130 (Cancelled)

131. (Currently Amended) ~~An arithmetic~~ A coding apparatus for coding input image data in a predetermined signal format by dividing said image data into block units and by carrying out orthogonal ~~transform~~ transformation in said block units ~~or for subjecting coded data to inverse orthogonal transform and signal format conversion to obtain image data for decoding~~ at a time when data output value ~~Y0, i.e.,~~ X0 + X1 , and data output value ~~Y1, i.e.,~~ X0 – X1 , are generated from two input data values X0 and X1 by at least a function of said orthogonal ~~transform~~ transformation ~~or said inverse orthogonal transform~~, said apparatus comprising:

~~first, a subtraction means for subtracting said X1 from said X0 to generate new X0,~~

~~second, a twice value generating means for generating new X1 being twice the value of said X1, and~~

~~third, an addition means for adding said new X0 to said new X1 to generate newer X1, wherein~~

~~said newer X1 is used as output value Y0, and said new X0 is used as output value Y1~~

a register A into which said X0 value is stored;

a register B into which said X1 value is stored;

a first subtraction means for subtracting said X1 value from said X0 value to obtain a new X0 value and store it into said register A, and outputting said new X0 value as a difference between said X1 value and said X0 value;

a shift register for shifting said X1 value used as a binary number by one bit to a MSB side to obtain a new X1 value and store it in said register B; and

addition means for adding said new X0 value to said new X1 value to obtain a further new value X1 and outputting said further new value X1 as a sum of said new X0 value and said new X1 value.

132 - 134 (Cancelled)